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***Abstract*—In this contribution a 44.5 dBm gallium nitride (GaN) based Doherty amplifier for a center frequency of 4900 MHz is presented. The developed Doherty amplifier uses an unsymmetrical power division and offset lines for optimization of the load modulation over the dynamic output range. Various drain supply voltages of the carrier and the peak amplifier are used to optimize the gain. Furthermore, the error vector magnitude (EVM) and the adjacent channel leakage ratio (ACLR) are reduced by using a memoryless digital predistortion (DPD) based on lookup table (LUT) model. All this design strategies improve the linearity of the Doherty amplifier.**

I. Introduction

Simple power amplifier structures based on a single transistor can achieve their highest efficiency only at the maximum output power. The amplifications of signals with high peak-to-average power ratios (e.g., orthogonal frequency division multiplexing (OFDM)) with power amplifiers, based on a single transistor, is therefore less efficient. This can be enhanced with, e.g., an envelope tracking amplifier, where the drain voltage is continuously adjusted to achieve the maximum efficiency corresponding to output power [1]. Another possible approach to enhance the efficiency is the Doherty amplifier [1] and [2]. Doherty amplifiers have been discussed in a large number of publications for various applications, e.g. [1], [3]. For the used center frequency of $f_0 = 4900\,\mathrm{MHz}$, unsymmetrical power division and various drain supply voltage exist no further publication. To match the linearity requirements, which is necessary to transmit a 64-QAM-OFDM signal, a memoryless DPD is used.

In this work a Doherty power amplifier, based on GaN high electron mobility transistors (HEMT), is used for an efficiency enhancement over a large range of output power. Furthermore, an unsymmetrical power division, offset lines and different drain bias supply voltages are used to optimize the load modulation and the gain over the back-off range. First, a short introduction to the theoretical background of the Doherty amplifier is presented. In Section III the design of the Doherty amplifier is shown. Subsequently in Section IV, measurement results for a continuous wave (CW) and a 20 MHz 64-QAM-OFDM signal of the developed Doherty amplifier with and without DPD are discussed.

II. Theoretical Background Doherty Amplifier

The classical Doherty architecture according to [2] consists of two single amplifiers (see Fig. 1), the so called carrier and peak amplifier. The power divider splits the input signal into both of them. At the output, both amplifiers are connected over a combing network to a common load equal to $Z_L = 50\,\Omega$, whereas the combing network consists of an impedance inverter and a matching network.

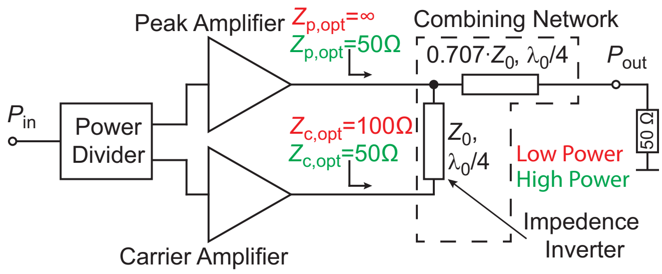

Fig. 1. Block diagram of a Doherty power amplifer.

The impedance inverter is usually implemented as a microstrip-line with the characteristic impedance of optimal load impedance of the carrier and the peak amplifier $Z_{\mathrm{opt}} = Z_{\mathrm{c,opt}} = Z_{\mathrm{p,opt}}$ and a phase shift of uneven multiples of $90\,°$. The performance of the Doherty amplifier can be divided into two parts, the low power (LP) and the high power (HP) range.

In the low power range, only the carrier amplifier is active, due to the specific bias point of the peak amplifier. Hence, the input voltage of the peak amplifier is smaller than its threshold voltage. In this range the carrier amplifier is terminated with $Z_{\mathrm{c,opt}} = 100\,\Omega$ and the peak amplifier provides $Z_{\mathrm{p,opt}} = \infty$ due to the combining network for the center frequency f_0.

In the high power range, the efficiency only varies by a small amount depending of the back-off, whereas a slight efficiency drop exists dependent on the load modulation of the carrier amplifier and the power ratio of the carrier and the peak amplifier [4].

The optimal load of the carrier amplifier $(2 \cdot Z_{\mathrm{c,opt}}\ (\mathrm{LP}))$ decreases for increasing output power $(Z_{\mathrm{c,opt}}\ (\mathrm{HP}))$, because the peak amplifier begins to amplify. In this case, for maximal output power, both amplifiers have the same optimal load impedance $Z_{\mathrm{p,opt}} = Z_{\mathrm{c,opt}} = 50\,\Omega$. This load modulation of the carrier amplifier enhances the overall efficiency of the Doherty amplifier.

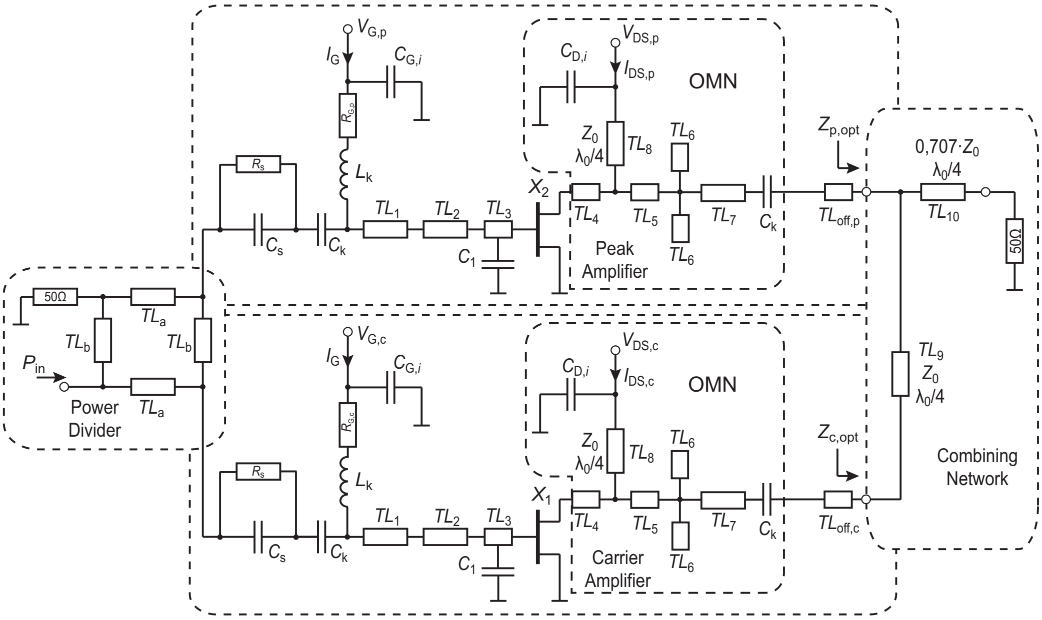

Fig. 2. Schematic of the developed Doherty amplifier.

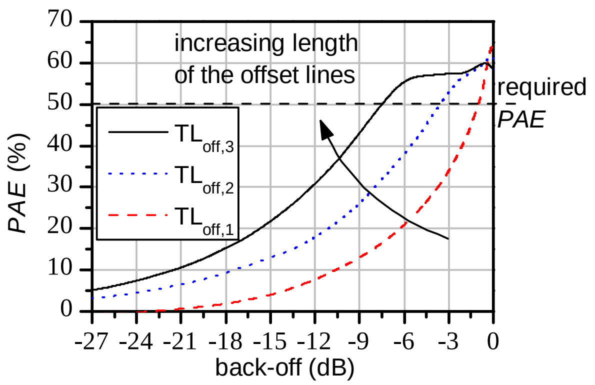

Fig. 3. Simulated *PAE* versus back-off for various offset lines lengths.

III. Design of a Doherty Amplifier for C-Band Applications

The schematic of the developed Doherty power amplifier for a center frequency of $f_0 = 4900\,\mathrm{MHz}$ is shown in Fig. 2. Both, the carrier and the peak amplifier, uses the same GaN HEMT CGH55015 from Wolfspeed.

TABLE I
Length of the Offset Lines

$TL_{off,i}$	peak amplifier $TL_{off,p}$	carrier amplifier $TL_{off,c}$	back-off over required *PAE*
1	$0 \cdot \lambda_{f_0}$	$0 \cdot \lambda_{f_0}$	≈1.2 dB
2	$0.065 \cdot \lambda_{f_0}$	$0.089 \cdot \lambda_{f_0}$	≈3.5 dB
3	$0.269 \cdot \lambda_{f_0}$	$0.196 \cdot \lambda_{f_0}$	≈7.5 dB

The unsymmetrical power division is a common method to overcome the effect of lower gain of the peak amplifier [5]. The power divider from Fig. 1 is designed as unsymmetrical branch line hybrid coupler [6]. The 90° phase shift between the coupler output signals compensates the 90° phase shift of the impedance inverter. The power division ratio has been chosen in this design, so that the peak amplifier gets less power than the carrier amplifier. Through this power division and a higher drain bias voltage $V_{\mathrm{DS,p}}$ the peak amplifier can be operated near the Class-B condition and as a consequence thereof, provides a higher gain.

Both amplifiers are matched to $Z_{\mathrm{c,opt}} = Z_{\mathrm{p,opt}} = 50\,\Omega$ for maximum output power through the microstrip lines TL_4, TL_5 and TL_7 of the output matching network (OMN). The termination of the second harmonic is realized with a $\lambda_{f_0}/4$-microstrip line (TL_8), short-circuited by the capacitance $C_{\mathrm{D},i}$. In addition, the $\lambda_{f_0}/4$-microstrip line is also used for the supply of the drain source voltage $V_{\mathrm{DS,P}}$ and $V_{\mathrm{DS,C}}$. Two $\lambda_{f_0}/12$ open-circuited stubs TL_6 are placed behind the microstrip line TL_5 to provide a short for the third harmonic at the internal current source plane.

For optimization of the load modulation the offset lines ($\mathrm{TL}_{\mathrm{off,p}}$ and $\mathrm{TL}_{\mathrm{off,c}}$) are integrated between the output matching network (see Fig. 2) and the impedance inverter. The detailed theoretical behaviour of this design strategy is described, e.g., in [7] and [8].

For the center frequency of $f_0 = 4900\,\mathrm{MHz}$ various lengths for the offset lines are investigated. The influence of the line length for the load modulation respectively fot the *PAE* behavior over the back off range are presented in Fig. 3. The optimization target is a *PAE* higher than 50 % over a large back-off range. Table I shows the investigated offset lines lengths. The best result for the *PAE* is achieved by the $\mathrm{TL}_{\mathrm{off,3}}$ length, which corresponds to a back-off range of 7.5 dB with a *PAE* higher than 50 %.

With this offset lines length the requirements to efficiency enhancement in the back-off range of a modern communications system are fulfilled.

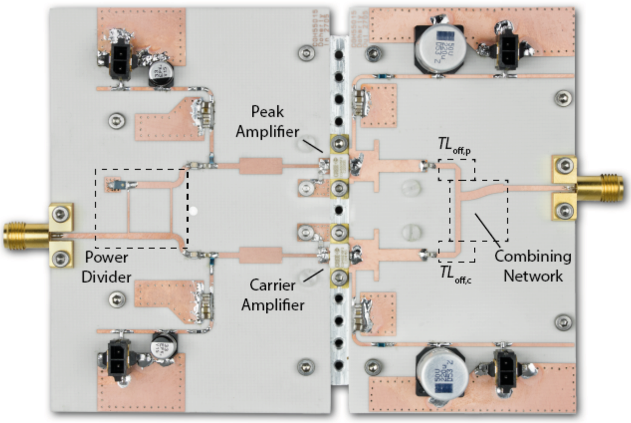

Fig. 4. Photo of the developed Doherty power amplifier.

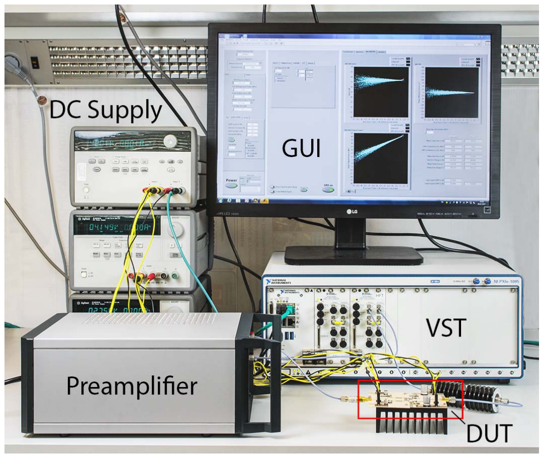

Fig. 6. Measured setup for the DPD based on a NI vector signal transceiver.

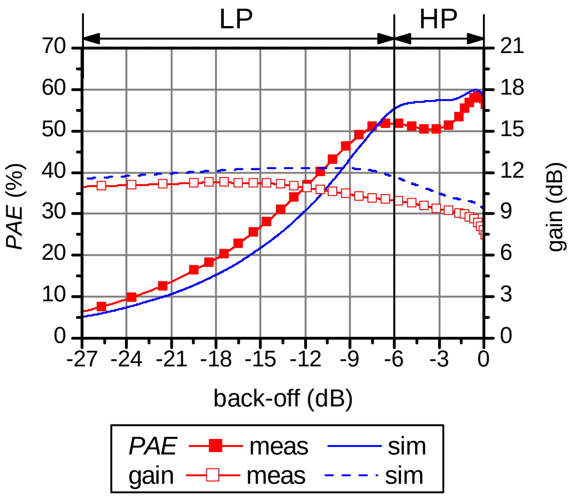

Fig. 5. Measured and simulated *PAE* and gain versus back-off for the offset line $\mathrm{TL}_{\mathrm{off},3}$.

IV. Realization of Linear and Efficient Doherty Amplifier for C-Band Applications

In this section, the realization (see Fig. 4) and measurement results of the Doherty power amplifier based on the previous section are presented.

The power amplifier is fabricated on a Rogers RO4003 laminate, with a permittivity of $\epsilon_{\mathrm{r}} = 3.55$ and a thickness of $h = 508\,\mu\mathrm{m}$. It is mounted on an aluminum plate for more mechanical stability. The chosen gate bias voltages are $V_{\mathrm{GS,c}} = -2.75\,\mathrm{V}$ and $V_{\mathrm{GS,p}} = -4.10\,\mathrm{V}$ and the drain bias voltages are $V_{\mathrm{DS,c}} = 30\,\mathrm{V}$ and $V_{\mathrm{DS,p}} = 40\,\mathrm{V}$. In this configuration the power amplifier achieves a maximum output power of $P_{\mathrm{out}} = 44.5\,\mathrm{dBm}$. In the following the Doherty amplifier is characterized with a CW and a 64-QAM-OFDM signal.

A. Continuous Wave Signal

The measured results for the *PAE* and the gain are shown in Fig. 5 for a CW signal at the center frequency f_0. Measurement and simulation show a sufficient agreement over the back-off range. The measured *PAE*-envelope shows an efficiency at 7.5-dB-back-off of 50 %. Nevertheless, due to the tolerance of the fabrication process for the combining network respectively the offset lines the efficiency at 7.5-dB-back-off is lower than at 0-dB-back-off, which can be justified with the results of the investigation in Section III.

Furthermore, the measured gain in Fig. 5 shows a smaller gain variation over the back-off range compared to the simulation. The unsymmetrical power division and the higher drain voltage supply of the peak amplifier should be further optimized for higher gain in the HP range.

B. 64-QAM-OFDM Signal

The amplifier is part of a transmitter for a non commercial communication system with high data rate. A 64-QAM-OFDM modulation scheme is used and the signal bandwith is 20 MHz. Therefore, high requirements with respect to the linearity and the efficiency are necessary [9]. The high efficiency over a large back-off range is fulfilled with the proposed Doherty amplifier, but the linearity should be optimized by using a digital predistortion (DPD).

The used setup is based on a National Instrument (NI) vector signal transceiver (VST) PXIe-5646R with a possible bandwidth of 200 MHz and a Class A preamplifier with approximately 44 dB gain (see Fig. 6). For controlling the VST basic functions from NI are used. The memoryless lookup table (LUT) model, which is used for linearization of the Doherty amplifier, is realized in MATLAB as well as all required calculation for the LUT. The signal generation, modulation and demodulation are realized with basic MATLAB and LABVIEW functions. The possibility to control all parameters of the signal chain are significant to evaluate their influence of the DPD performance. To interpret the performance of the DPD the gain curve (AM-AM), the phase (AM-PM), the adjacent channel leakage ratio (ACLR) and as well as the EVM without and with DPD are used. In the next step the developed DPD will be realized on a Xilinx ZYNQ-7000 FPGA board which acts as a baseband processor for the 9361 Analog Devicse RF Transceiver as RF front end.

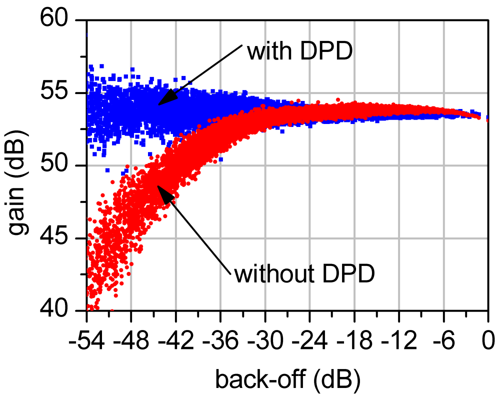

Fig. 7. Measured gain curve (AM-AM) without and with memoryless DPD.

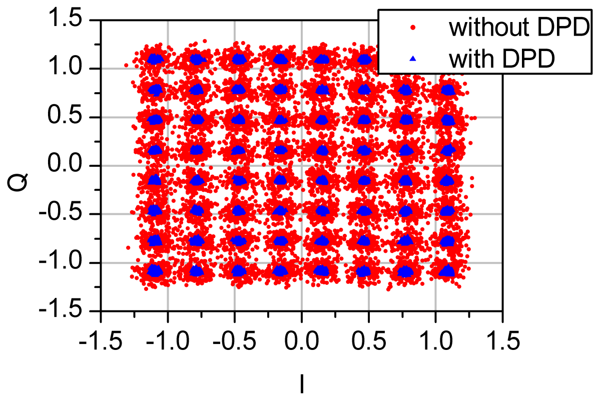

Fig. 9. Measured 64-QAM constellation without and with memoryless DPD.

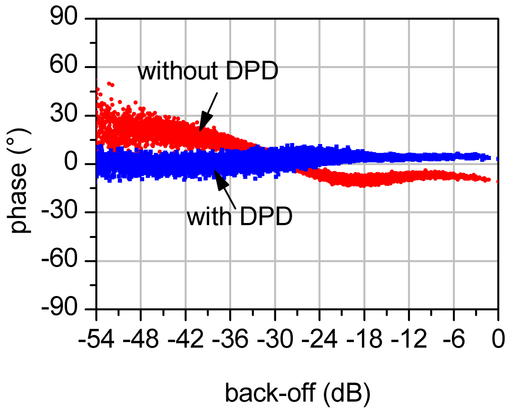

Fig. 8. Measured phase (AM-PM) without and with memoryless DPD.

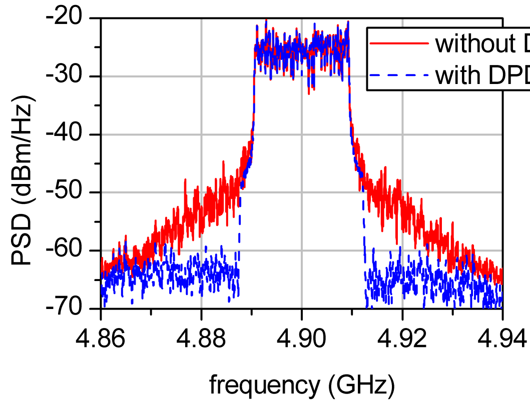

Fig. 10. Measured power spectral density of a 20 MHz 64-QAM-OFDM signal without and with memoryless DPD.

The gain curve (AM-AM) (included the gain of the preamplifier) and the phase (AM-PM) without and with digital predistortion over the back-off range are presented in Fig. 7 and Fig. 8. These results show improved gain and phase linearity with the memoryless DPD. The 64-QAM constellation (see Fig. 9) shows a reduction of the EVM from 8.8 % without DPD to 2.0 % with the memoryless DPD. Furthermore, the power spectral density (PSD) in Fig. 10 shows a reduction of the ACLR. Summarising, the memoryless DPD linearized the used Doherty amplifier for the intended application of transmitting a 64-QAM-OFDM signal by reduction of the EVM to 2.0 %.

V. Conclusion

In this work a linearized and efficient GaN HEMT based Doherty amplifier for C-Band communication application is introduced. The load modulation is optimized through offset-lines in the output matching networks, a input power divider with unsymmetrical power divison and different supply voltages of the carrier and peak amplifier. With the proposed Doherty amplifier the efficiency requirements for modern communication systems are fulfilled. For enhancing the linearity of the Doherty amplifier a memoryless digital predistortion is used, which reduces the out-of-band and in-band distortion as shown through a reduction of the EVM and the ACLR.

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